



53/63RS881/A

High Performance 1024x8 Registered PROM

FEATURES/BENEFITS

- Edge triggered "D" registers
- Synchronous and asynchronous enables
- Versatile 1:16 initialization words
- 8-Bit-wide In 24-pin SKINNYDIP® package for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA IOL output drive capability
- Reliable titanium-tungsten fuses (TIW), with programming yields typically greater than 98%

APPLICATIONS

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™) 10 Inputs, 8 Registered Outputs, 1024 product terms

DESCRIPTION

The 53/63RS881 and 53/63RS881A are 1Kx8 PROMs with on-chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start-up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous (\bar{E}) and synchronous (\bar{ES}) enables are LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting \bar{E} to a HIGH or if \bar{ES} is HIGH when the rising clock edge occurs. When V_{cc} power is first ap-

plied, the synchronous enable flip-flop will be in the set condition, causing the outputs to be in the high-impedance state.

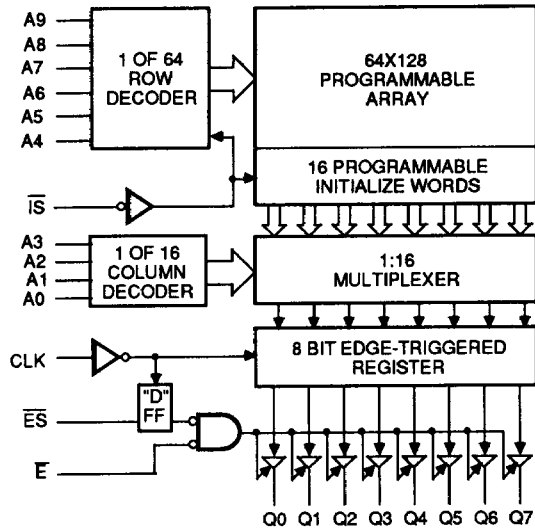
The flexible initialization feature allows start-up and time-out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE (\bar{IS}) pin LOW, one of the sixteen column words (A3-A0) will be set in the output registers independent of the row addresses (A9-A4). The unprogrammed state of \bar{IS} words are LOW, presenting a CLEAR with \bar{IS} pin LOW. With all \bar{IS} column words (A3-A0) programmed to the same pattern, the \bar{IS} function will be independent of both row and column addressing and may be used as a single pin control. With all \bar{IS} words programmed HIGH, a PRESET function is performed.

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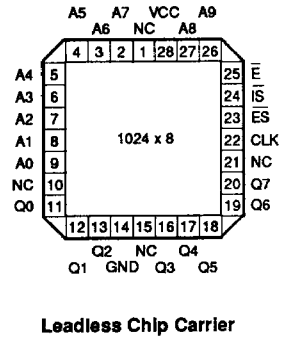
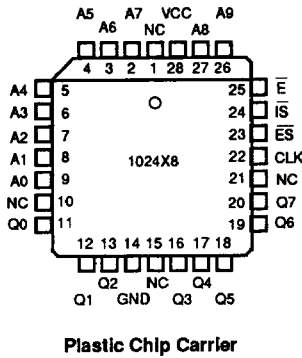
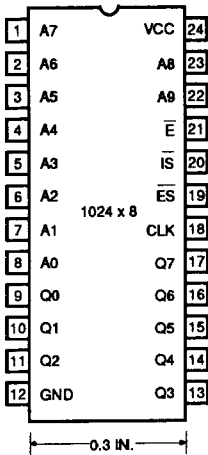
SELECTION GUIDE

| Memory | | Package | | Performance | Part Number | |
|--------|--------------|------------|---------|-------------|--------------|-----------------|
| Size | Organization | Pins | Type | | 0°C to +75°C | -55°C to +125°C |
| 8K | 1024x8 | 24 (28) | CD 3024 | Enhanced | 63RS881A | 53RS881A |
| | | | PD 3024 | | | |
| | | | PL 028 | Standard | 63RS881 | 53RS881 |
| | | | CL 024 | | | |
| | | | CFM 024 | | | |

BLOCK DIAGRAM



PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Operating Programming

| | | |
|--------------------------------|-----------------------|------|
| Supply voltage V_{CC} | -0.5 V to 7 V | 12 V |
| Input voltage | -1.5 V to 7 V | 7 V |
| Input current | -30 mA to +5 mA | |
| Off-state output voltage | -0.5 V to 5.5 V | 12 V |
| Storage temperature | -65°C to +150°C | |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect reliability. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

Operating Conditions

| Symbol | Parameter | Typ† | Military†† | | | | Commercial | | | | Unit |
|------------------------|--|------|------------|-----|---------|-----|------------|------|---------|------|------|
| | | | 53RS881A | | 53RS881 | | 63RS881A | | 63RS881 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_w | Width of clock (High or Low) | 10 | 20 | | 20 | | 20 | | 20 | | ns |
| $t_{s(A)}$ | Setup time from address to clock | 25 | 40 | | 45 | | 30 | | 35 | | ns |
| $t_{s(ES)}$ | Setup time from \overline{ES} to clock | 8 | 15 | | 15 | | 15 | | 15 | | ns |
| $t_{s(\overline{IS})}$ | Setup time from \overline{IS} to clock | 20 | 30 | | 35 | | 25 | | 30 | | ns |
| $t_{h(A)}$ | Hold time address to clock | -5 | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{h(ES)}$ | Hold time (\overline{ES}) | -3 | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{h(\overline{IS})}$ | Hold time (\overline{IS}) | -5 | 0 | | 0 | | 0 | | 0 | | ns |
| V_{CC} | Supply voltage | 5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.75 | 5.25 | 4.75 | 5.25 | V |
| T_A | Operating temperature* | 25 | -55 | 125 | -55 | 125 | 0 | 75 | 0 | 75 | °C |

* This is defined as the instant-on case temperature.*

† Typicals at 5.0 V V_{CC} and 25°C T_A .

†† Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Electrical Characteristics Over Operating Conditions. For APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted.

| Symbol | Parameter | Test Conditions | | Min | Typ† | Max | Unit |
|-----------|-------------------------------|---|----------------------------|----------------------------|------|-------|---------------|
| V_{IL} | Low-level input voltage** | | | | | 0.8 | V |
| V_{IH} | High-level input voltage** | | | 2.0 | | | V |
| V_{IC} | Input clamp voltage | $V_{CC} = \text{MIN}$ | $I_I = -18 \text{ mA}$ | | | -1.2 | V |
| I_{IL} | Low-level input current | $V_{CC} = \text{MAX}$ | $V_I = 0.4 \text{ V}$ | | | -0.25 | mA |
| I_{IH} | High-level input current | $V_{CC} = \text{MAX}$ | $V_I = V_{CC} \text{ MAX}$ | | | 40 | μA |
| V_{OL} | Low-level output voltage | $V_{CC} = \text{MIN}$ | $I_{OL} = 16 \text{ mA}$ | | | 0.5 | V |
| V_{OH} | High-level output voltage | $V_{CC} = \text{MIN}$ | Com | $I_{OH} = -3.2 \text{ mA}$ | 2.4 | | V |
| | | | Mil | $I_{OH} = -2 \text{ mA}$ | | | |
| I_{OZL} | Off-state output current | $V_{CC} = \text{MAX}$ | $V_O = 0.4 \text{ V}$ | | | -40 | μA |
| I_{OZH} | | | $V_O = 2.4 \text{ V}$ | | | 40 | |
| I_{OS} | Output short-circuit current* | $V_{CC} = 5 \text{ V}$ | $V_O = 0 \text{ V}$ | | -20 | -90 | mA |
| I_{CC} | Supply current | $V_{CC} = \text{MAX}$. All inputs TTL. All outputs open. | | | 130 | 180 | mA |

* Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

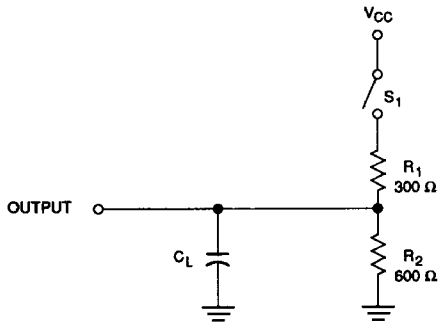
** V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

† Typicals at 5.0 V V_{CC} and 25°C T_A .

Switching Characteristics Over Operating Conditions and using Standard Test Load. For APL Products, Group A, subgroups 9, 10, 11 are tested unless otherwise noted.††

| Symbol | Parameter | Typ† | Military | | | | Commercial | | | | Unit |
|-----------|-------------------------------------|------|----------|-----|---------|-----|------------|-----|---------|-----|------|
| | | | 53RS881A | | 53RS881 | | 63RS881A | | 63RS881 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{CLK} | Clock to output Delay | 10 | | 20 | | 25 | | 15 | | 20 | ns |
| t_{ESA} | Clock to output access time (ES) | 18 | | 30 | | 35 | | 25 | | 30 | ns |
| t_{ESR} | Clock to output recovery time (ES) | 17 | | 30 | | 35 | | 25 | | 30 | ns |
| t_{EA} | Enable to output access time (E) | 18 | | 30 | | 35 | | 25 | | 30 | ns |
| t_{ER} | Disable to output recovery time (E) | 17 | | 30 | | 35 | | 25 | | 30 | ns |

†† Subgroups 7 and 8 apply to Functional tests.



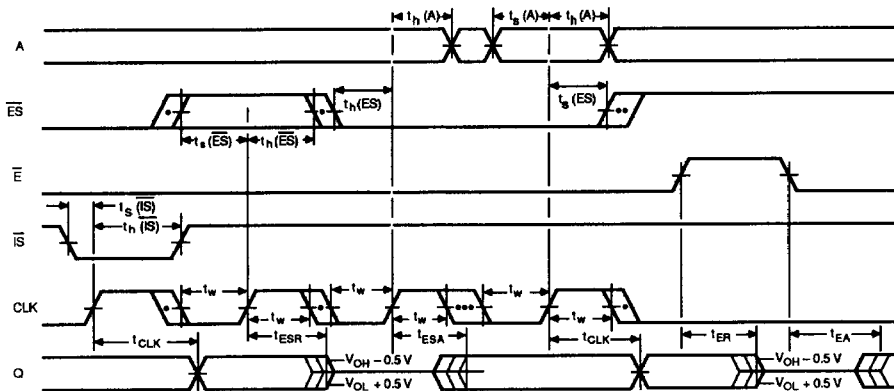
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Figure 1. Switching Test Load

| WAVEFORM | INPUTS | OUTPUTS |
|----------|---------------------------------|--|
| | DON'T CARE: CHANGE PERMITTED | CHANGING: STATE UNKNOWN |
| | NOT APPLICABLE | CENTER LINE IS HIGH IMPEDANCE STATE |
| | MUST BE STEADY | WILL BE STEADY |

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Figure 2. Definition of Timing Diagrams



- NOTES:
1. INPUT PULSE AMPLITUDE 0 V TO 3.0 V.
 2. INPUT RISE AND FALL TIMES 2-5 ns FROM 0.8 V TO 2.0 V.
 3. INPUT ACCESS MEASURED AT THE 1.5 V LEVEL.
 4. t_{AA} IS TESTED WITH SWITCH S_1 CLOSED, $C_L = 30$ pF AND MEASURED AT 1.5 V OUTPUT LEVEL.
 5. t_{EA} AND t_{ESA} ARE MEASURED AT THE 1.5 V OUTPUT LEVEL WITH $C_L = 30$ pF. S_1 IS OPEN FOR HIGH IMPEDANCE TO "1" TEST, AND CLOSED FOR HIGH IMPEDANCE TO "0" TEST.
- t_{ER} AND t_{ESR} ARE TESTED WITH $C_L = 5$ pF. S_1 IS OPEN FOR "1" TO HIGH IMPEDANCE TEST, MEASURED AT $V_{OH} - 0.5$ V OUTPUT LEVEL; S_1 IS CLOSED FOR "0" TO HIGH IMPEDANCE TEST, MEASURED AT $V_{OL} + 0.5$ V OUTPUT LEVEL.

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Figure 3. Definition of Waveforms